SPECIFICATION

Please replace the paragraph beginning on page 6, line 17, with the following amended paragraph:

For the case in which the data for the prefetch addresses, the addresses in addition to the address that came from DSP core 18 as a request for data, has not a arrived and another request, different from the prefetch addresses, has arrived then there is both a miss in cache 24 and a prefetch miss. This results in fetch unit 22 terminating the outstanding prefetches, which by its nature also prevents the entry of the prefetched data onto the program data bus, but there may be memory types in external memory that do not allow requests for data to be terminated after they have been received. If that is the case, the automatic generation of the prefetch addresses in that sequence is terminated, but the data that is received is loaded in cache 24. This provides for a partial line fill. A line, such as line 34, is then only filled to the extent of the prefetches until the next fetch address that is not also a prefetch address is received. Thus, prefeteched data that is received is stored in the cache without waiting for any previously received prefetched data being placed on the program data bus.

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